Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1. (Currently Amended) A semiconductor device comprising:

[[an]] anode ~~driver~~ drivers and [[a]] cathode ~~driver~~ drivers ~~laid out equally in~~ arranged in a plurality of discrete groups on a chip; and

discrete memory portions ~~connected~~ coupled to the drivers, each of the memory ~~portion arranged equally in the vicinity of each of the driver~~ portions associated with one or more of the groups,

wherein the semiconductor device is made in one chip with the drivers and memory portions, and

wherein the groups are located along the periphery of the chip.

2. (Canceled)

3. (Original) The semiconductor device according to claim 1,

wherein the drivers connected to the memory portions are placed face to face at right and left positions or high and low positions of the chip, and each of the memory portions is arranged at center portion of the chip.

4. (Original) The semiconductor device according to claim 1, wherein each of the drivers includes a plurality of output regions corresponding to one bit constituting an output bit group, the semiconductor device further comprising a dummy pattern having the same shape as the output bit formed to be adjacent to the end portion of the output bit group.

5. (Original) The semiconductor device according to claim 4, wherein the dummy pattern is formed at an empty space in a region where a plurality of output bits are arranged.

6. (Original) The semiconductor device according to claim 4, wherein number of outputs of the dummy pattern formed at a region where output bit groups are adjacent each other is less than number of outputs of the dummy pattern formed at a region where output bit groups are not adjacent each other.

7. (Original) The semiconductor device according to claim 4, wherein the dummy pattern has the same shape as a wiring for gate electrode.

8. (Currently Amended) A semiconductor device for drivers made in one chip comprising:

output regions corresponding to one bit arranged to constitute discrete output bit groups; and

discrete memory portions coupled to associated discrete output bit groups,

wherein a plurality of the discrete output bit group are arranged at a periphery portion ~~in~~ of the chip.

9. (Currently Amended) The semiconductor device according to claim 8 further comprising wirings connected to each of the output bit groups arranged at the periphery portion arranged to ~~circle fitting~~ fit the shape of the chip.

10. (Currently Amended) The semiconductor device according to claim 8, further comprising:

drivers having the output regions corresponding to one bit to constitute the output bit groups;

~~memory portions;~~ and

wirings connected to each of the output bit groups,

wherein the drivers are arranged at a periphery portion in the chip in a state that the drivers are grouped by every desired output bit group,

wherein the wirings connected to each of the output bit groups arranged at the periphery portion is arranged to ~~circle fitting~~ fit the shape of the chip,

wherein the semiconductor device constitutes a display driver.

11. (Original) The semiconductor device according to claim 10, wherein the drivers includes an anode driver and a cathode driver, and the drivers are arranged at periphery portion in the chip in a state that one of the anode driver and the cathode driver is grouped by every desired output bit group.

12. (Original) The semiconductor device according to claim 9, wherein the wirings include a power source line and a signal line.

13. (Original) The semiconductor device according to claim 10, wherein ~~the~~ each output bit group is arranged to surround the memory portions at the periphery portion.

14. (Original) The semiconductor device according to claim 10, further comprising a dummy pattern having the same shape as the output bits formed to be adjacent ~~to~~ the end portion of the output bit group.

15. (Original) The semiconductor device according to claim 14, wherein the dummy pattern is formed at an empty space in a region where a plurality of output bits are arranged.

16. (Currently Amended) The semiconductor device according to claim 14, wherein the number of outputs of the dummy pattern formed at a region where output bit groups are adjacent

each other is less than the number of outputs of the dummy pattern formed at a region where output bit groups are not adjacent each other.

17. (Original) The semiconductor device according to claim 14, wherein the dummy pattern has the same shape as a wiring for gate electrode.

18. (New) The semiconductor device of claim 1, wherein the segments are arranged around the memory portions.

19. (New) The semiconductor device of claim 1, wherein the wirings of the memory portions to the drivers are arranged symmetrically on the chip.